REMARKS

The Examiner's Final Action mailed on December 19, 2003 has been received and its contents carefully considered. Reconsideration of the final rejections presented therein is respectfully requested for at least the following reasons.

Initially, it is noted that the Examiner's Action has repeated the rejections presented in the earlier Office Action. As such, this Request incorporates by reference the arguments made in the Amendment filed October 31, 2003, which are still deemed to be pertinent to the rejections at hand.

The Examiner has rejected claims 1, 4 and 8 as being anticipated by *Marrs et al.* (USP 5,583,378). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 U.S.C. §102 only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principle of inherency.

Applicant's independent claim 1 recites at least the following features, none of which are disclosed by the cited reference:

1) a common adhesive layer, which is in direct contact with and over a principal surface of a heat spreader and is in direct contact with both a semiconductor chip and a wiring board so as to bond both the semiconductor chip and the wiring board to the heat spreader;

2) so that a heat transfer effect between the semiconductor chip and the heat spreader is about equal to a heat transfer effect between the wiring board and the heat spreader; and

3) a portion of the heat spreader within an opening that is not covered by the semiconductor chip is completely covered by the adhesive layer.

The Examiner's Action, in the Response to Arguments, has clarified the Examiner's interpretation of the cited reference. In particular, the Action states that adhesive layers 210 and 206 are in direct contact with each other. However, as will be explained in the paragraphs that follow, it is believed that the Examiner's Action has misinterpreted the cited reference, and that these layers are not in contact with each other, as alleged in the Action.

To facilitate Applicant's explanation of the cited reference, and to further the Examiner's understanding of the cited reference, Applicant has modified Figure 2D of the cited reference, to label the constituent elements in a more easy to comprehend manner. Please note that Figure 2D is directed to a different embodiment than the embodiment relied upon by the Action, as shown in Figure 2A; nevertheless, the features relied upon by the Action that are shown in Figure 2A are likewise shown in a similar manner in Figure 2D.

As shown in Applicant's modified Figure 2D, a thermal conductor 204 is provided. A lower surface of the thermal conductor has an optional adhesion layer 228 formed thereon. On the left hand side of the drawing, the chip 202 is adhered to the optional adhesion layer 228 using an adhesive 206. On the right hand side of the drawing, the conductive trace 212 is adhered to the optional adhesion layer 228 using an adhesive

layer 210. As shown, the adhesive 206 is separated from the adhesive layer 210 by a space. The Figure shows that the encapsulant material 226 is in direct contact with the optional adhesion layer 228 in this space.

The Examiner's Action has apparently mistaken the optional adhesion layer 228 for the adhesive layer 210. Applicant admits that Figure 2A is confusing and poorly labeled, but will show that Applicant's interpretation of the Figures is the correct interpretation.

That is, it is initially noted that the reference states that adhesion layer 228 is formed on the surface of the thermal conductor 204, and enhances the adhesion of interconnection substrate 208 (i.e., conductive trace 212), chip 202 and encapsulant material 226 to the surface of the thermal conductor 204 (see column 8, lines 10-16). From this disclosure, it is clear that the adhesion layer 228 extends across the entire surface of the thermal conductor 204. However, there is only one layer illustrated that has this configuration. If this one layer were, in fact, the adhesive layer 210 as apparently presented by the Examiner's Action, then the drawings of the reference would fail to illustrate the adhesion layer 228. However, the reference makes clear that the adhesion layer 228 is illustrated. Moreover, if it was the adhesive layer 210 that extended across the entire surface of the thermal conductor 204, rather than the adhesion layer 228, then the drawings of the reference would fail to identify the layer shown in alternating dark/light lines, which is disposed immediately above the conductive trace 212. That is, this layer shown in alternating dark/light lines could not be the adhesion layer 228, since adhesion layer 228 is disclosed as also being under the chip 202 and over the encapsulant material 226. Since the layer shown in

alternating dark/light lines is not under the chip 202 or over the encapsulant material 226, one can logically conclude that this layer cannot possibly be the adhesion layer 228, but is instead the adhesive layer 210.

This reference also teaches that, in one embodiment, the surface of the thermal conductor 204 is exposed at a bottom of the well region 236, i.e., the region adjacent to the chip 202 (column 8, lines 22-26). Since this reference also teaches that the adhesion layer 228 is optional, one can logically conclude that this embodiment proposes eliminating the adhesion layer 228, to expose the surface 205. However, if the adhesive layer 210 is formed along the entire surface of the thermal conductor 204, as presented by the Examiner's Action, then the surface would never be exposed, even with the elimination of the optional adhesive layer 228. Thus, one can also logically conclude that the adhesive layer 210 is not formed along the entire surface of the thermal conductor 204, but is instead only formed between the conductive trace 212 and the thermal conductor 204. That is, if the adhesive layer 210 was formed along the entire surface, as apparently proposed by the Examiner's Action, then the surface would not ever be exposed, even with the elimination of the optional adhesion layer 228.

As such, from the foregoing, it is clear that the adhesive layer 210 is not disposed in direct contact with the adhesive 206, as presented by the Examiner's Action.

In view of the above, and as presented in detail in Applicant's last-filed Amendment, the cited reference does not disclose a common adhesive layer, which is in direct contact with and over a principal surface of a heat spreader and is in direct contact with both a semiconductor chip and a wiring board so as to bond both the semiconductor chip and the wiring board to the heat spreader, as recited in claim 1. Nor does the cited

reference disclose that a heat transfer effect between the semiconductor chip and the heat spreader is about equal to a heat transfer effect between the wiring board and the heat spreader, as recited in claim 1. Further, the cited reference does not disclose that a portion of the heat spreader within an opening that is not covered by the semiconductor chip is completely covered by the adhesive layer, as recited in claim 1.

Moreover, Applicant's independent method claim 4 is submitted to be patentably distinguishable over the cited reference for reasons similar to those given above with respect to independent claim 1. It is thus requested that this rejection be withdrawn, and that these claims be allowed.

Further, dependent claim 8 is submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which this claim depends, as well as for at least the following additional reason.

Claim 8 recites that the common adhesive layer covers the entire principle surface of the heat spreader. In contrast, and as noted above, the cited reference teaches that the adhesive layer 210 is disposed only between the conductive trace 212 and the thermal conductor 204, whereas the adhesive 206 is disposed only between the chip 202 and the thermal conductor 204. However, the area between the chip 202 and the conductive trace 212 is free of any adhesive. Thus, the entire principal surface of the thermal conductor 204 is not covered by an adhesive layer, much less a common adhesive layer. As such, it is requested that this claim be allowed, and that this rejection be withdrawn.

The Examiner has further rejected claims 2 and 3 as being obvious over *Marrs et al.*, and further in view of *Yamagata et al.* (USP 5,828,127). As noted above,

Applicant's independent claim 1 is *prima facie* patentably distinguishable over *Marrs et al.* Moreover, *Yamagata et al.* only disclose providing a fin 19 which is attached utilizing an adhesive 20. This reference does not overcome the above-noted deficiencies of *Marrs et al.*, so that the resulting combination does not disclose or otherwise suggest the features recited within independent claim 1. As such, dependent claims 2 and 3 are submitted to be patentably distinguishable over the cited combination of references for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recited therein. It is requested that these claims be allowed and it is further requested that these rejections be withdrawn.

The Examiner has rejected claims 5 and 6 as being obvious over *Marrs et al.* in view of *Yamagata*, and further in view of *Shin* (USP 5,807,769). It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Independent claim 5 recites a method which includes connecting electrodes of a semiconductor chip and a wiring board by metal thin wires; sealing a second adhesive layer and part of the semiconductor chip with a first encapsulating resin; and sealing the metal thin wires and the semiconductor chip with a second encapsulating resin after the first encapsulating resin has been cured. Per claim 5, the connecting of the electrodes is performed after sealing the second adhesive layer and part of the semiconductor chip with a first encapsulating resin, and before the sealing of the metal thin wires and the semiconductor chip with a second encapsulating resin. As disclosed by Applicant's specification, this claimed order of operations prevents voids from occurring, as

discussed on page 15, last three lines, through page 16, line 9. This claimed method is neither disclosed nor suggested by the cited references.

As acknowledged by the Examiner's Action, neither *Yamagata* nor *Marrs et al.* teach Applicant's claimed sealing operations. The Action thus relies on the teachings of *Shin* to overcome this admitted deficiency.

Shin discloses providing leads 4 around a chip 2, and connecting the leads to a chip using wires 5. After the leads are so connected, a first encapsulating part 6, 6a and a second encapsulating part 7a, 7b are deposited to seal the chip 2, wires 5 and the leads 4.

The Examiner's Action acknowledges that *Shin* does not teach Applicant's claimed order of operations. However, the Action states that the order of steps is irrelevant, and states that motivation for changing the order of the steps would be to provide greater flexibility to control the physical location of the wires and electrode.

However, it is noted that this alleged motivation appears to come entirely from the Examiner's own personal knowledge, since the Action makes no attempt to point out any motivation from the cited references for this change. Thus, this rejection appears to be either a hindsight attempt at reconstructing the cited references, which is impermissible under Section 103, or based on the Examiner's personal expertise. If this rejection is based on the Examiner's own knowledge and expertise, it is requested that the Examiner support this rejection with an affidavit. Alternatively, it requested that these claims be allowed, and that this rejection be withdrawn.

The Examiner has rejected claim 7 as being obvious over *Marrs et al.* in view of *Yamagata*, and further in view of *Shin and Ross* (USP 5,572,070). It is submitted that

this claim is patentably distinguishable over the cited references for at least the following reasons.

Claim 7 is directed to a method in which, after electrodes are connected to a wiring board by metal thin wires, a second adhesive layer and part of the semiconductor chip are sealed with an encapsulating resin. After the encapsulating resin has only partially cured, the metal thin wires and the semiconductor chip are sealed with more of the encapsulating resin. The advantages of this method are discussed in Applicant's specification. This claimed method is neither disclosed nor suggested by the cited references.

The Examiner's Action acknowledges that neither *Marrs et al,* nor *Yamagata*, nor *Shin* teach sealing metal thin wires and a semiconductor chip with more encapsulating resin after the first applied resin has partially cured, and relies on the teachings of *Ross* to overcome these admitted deficiencies.

Ross teaches a resin layer 20 that is used as a thermal conductive bridge between a die 13 and a lid 17. This reference discloses that a characteristic of this resin includes being in a partially cured state at lower temperatures, and is fully cured at higher temperatures.

However, *Ross* does not teach applying more resin after the first resin has partially cured, as recited in claim 7, and thus does not overcome the deficiencies of the other cited references. Moreover, claim 7 also recites that the second applied resin is the same as the first applied resin, and that the second applied resin is cured. If it is the Examiner's contention that the resin of *Ross* is never cured, then this resin could not be used as the second applied resin, as claim 7 requires that this resin be cured.

Moreover, the *Shin* patent teaches away from this claimed process, since *Shin* teaches that the first encapsulating part is cured before molding the second encapsulating part. Thus, there would have been no motivation for the combination proposed by the Examiner's Action, except in a hindsight attempt at recreating Applicant's claimed invention.

As such, it is submitted that claim 7 is *prima facie* patentably distinguishable over the combination of references relied upon by the Examiner, and it is requested that this claim be allowed. It is further requested that this rejection be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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